Date | 21 | 01 | 2023 | Subject Code | 21CS33 |

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Sir M. Visvesvaraya Institute of Technology
Bangalore 562 157
INTERNAL TEST PAPER

TEST NO : II | SEM : 3 | COURSE / BRANCH : BE / CSE | MAX. MARKS : 20 | DURATION : 60 Min

SUBJECT : Analog and Digital Electronics | Faculty Name : Mrs. Rekha B.N

Instructions: Answer any one Question from each PART

BL – Bloom's Taxonomy Levels (1- Remembering, 2- Understanding, 3 – Applying, 4 – Analyzing, 5 – Evaluating, 6 - Creating)

CO – Course Outcomes PO – Program Outcomes; PI – Performance Indicator

Q.No	Question	Marks	CO	BL	PO	PI
	PART A					
1	a) Implement following function using 8:1 Multiplexer $F(A, B, C, D) = \sum m(1, 2, 5, 6, 9, 12)$ also wirte VHDL CODE for 4:1 Mux	6	CO4 CO5	L3	PO2	2.5.1
	b) Implement full subtractor using 3:8 Decoder and NAND gates	4	CO4	L3	PO3	3.5.1
	OR					
2	a) Using Structural modelling style, write the VHDL code for FULL ADDER adding two 4-bit numbers	6	CO5	L3	PO2	2.5.1
	b) Realize the Following functions using PLA $F_1 = (A, B, C, D) = \sum m(1,2,4,5,6,8,10,12,14)$ $F_2 = (A, B, C, D) = \sum m(2,4,6,8,10,12,14,15)$.	4	CO4	L3	PO3	3.5.1
	PART B					
3	a) Construct the excitation table for JK and SR Flipflop. How SR Flipflop is converted to T-Flipflop	6	CO4	L3	PO3	3.8.3
	b) With a block diagram explain the working of a n-bit Parallel adder with accumulator	4	CO4	L2	PO2	2.6.3
	OR					
4	a) Draw the logic Diagram of JK Flipflop using NAND gates and illustrate its working	6	CO4	L3	PO3	3.8.3
	b) Obtain the characteristics equations of SR and JK Flipflop	4	CO4	L2	PO2	2.6.3

CO4: Explain Gates and Flipflops and make us designing different data processing circuits,registers and counters and compare types

CO4:Develop simple HDL PROGRAMS

Approved

Verified by QPSC Member

18/01/2023

Approved By HOD

18/1/23

DEPARTMENT OF COMPUTER SCIENCE & ENGG
Sir M. Visvesvaraya Institute of Technology
Hunasamaranahalli Off International Air Port Road,
Bangalore-562157.

Date 21 01 2023 Subject Code 21CS33

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Bangalore 562 157
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3	a) Derive the excitation table for JK and SR Flipflop. How SR Flipflop is converted to T-Flipflop	6	CO4	L3	PO3	3.8.3
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CO4: Explain Gates and Flipflops and make us designing different data processing circuits,registers and counters and compare types

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Do necessary corrections

18/01/2023

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II - Internal test Paper - 21CS33 — 21-01-2023

Scheme and Solution ADE — (1)

Staff :- Rekha B.N CSE A & B

1a. Implement function using 8:1 Mux — (4) m

$F(A,B,C,D) = \sum m(1,2,5,6,9,12)$

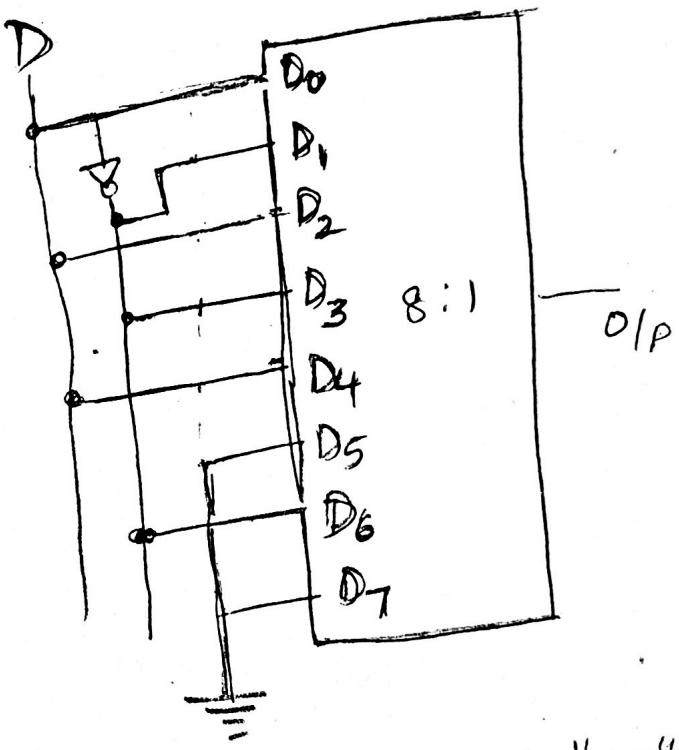
MEV table

A B C D	F	
0 0 0 0	0	D - D_0
0 0 0 1	1	
0 0 1 0	1	$\bar{D}$ - D_1
0 0 1 1	0	
0 1 0 0	0	D - D_2
0 1 0 1	1	
0 1 1 0	1	$\bar{D}$ - D_3
0 1 1 1	0	
1 0 0 0	0	D - D_4
1 0 0 1	1	
1 0 1 0	0	0 - D_5
1 0 1 1	0	
1 1 0 0	1	$\bar{D}$ - D_6
1 1 0 1	0	
1 1 1 0	0	0 - D_7
1 1 1 0	0	

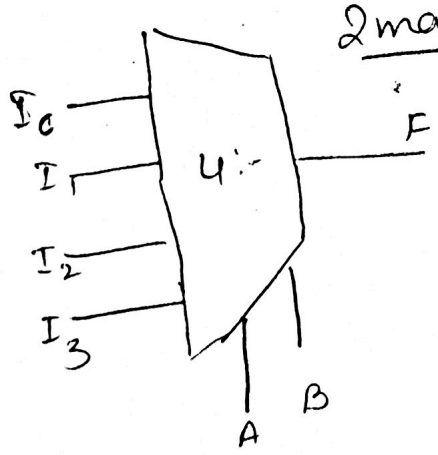
D - 0, 2, 4

$\bar{D}$ - 1, 3, 6

0 - 7, 5



2 marks



Sel <= A&B

with sel Select

F <- I_0 when "00"

F <= I_0 when A&B = "00"

else when A&B = "01"

else when A&B = "10"

else I_3;

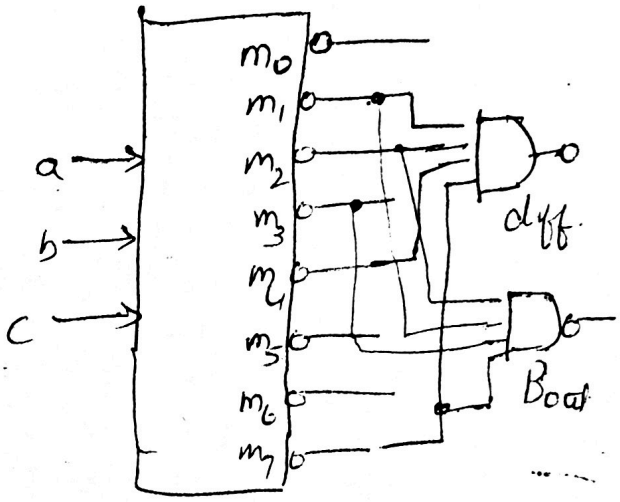
1 b. Full subtractor using 3:8 decoder and NAND gates

A	B	B_{in}	Diff	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$Diff = \Sigma m(1,2,4,7)$

$Bout = \Sigma m(1,2,3,7)$

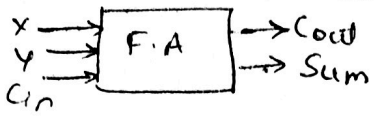
Diagram using decoder & Nandgate



2. a. Full adder

Full adder entity & Architecture – 2marks

Adder 4 entity & Architecture – 4marks




```
Entity FullAdder is
    port (x, y, Cin : in bit;
          Cout, Sum : out bit);
end FullAdder

Architecture Equations of FullAdder is
begin
    Sum <= x xor y xor Cin after 10ns;
    Cout <= (x and y) or (x and Cin) or (y and Cin)
                                        after 10ns
end Equations

Entity Adder4 is
  port (A, B : in bit_vector (3 downto 0); Ci : in bit -
        S : out bit_vector (3 downto 0); Co : out bit); -o/p
end Adder4;
architecture Structure of Adder4 is
Component FullAdder
    port (x, y, Cin : in bit ; -- Inputs
          Cout, Sum : out bit); -- Outputs
end component;
Signal C : bit_vector (3 downto 1);
begin -- instantiate four copies of full Adder
FA0 : FullAdder port map (A(0), B(0), Ci, C(1), S(0));
                port map (A(1), B(1), C(1), C(2), S(1))
```

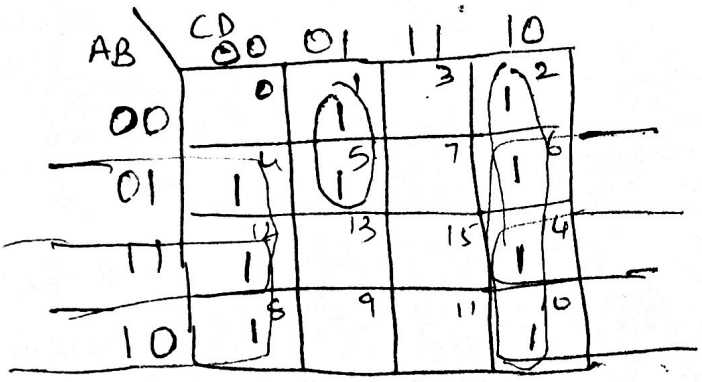
FA2 : Full Adder port map (A(2), B(2), C(2), C(3), S(2));
FA3 : Full Adder port map (A(3), B(3), C(3), Co, S(3));
end structure;

2.b Realizing PLA Circuits

K-map - 2marks

diagram - 2marks

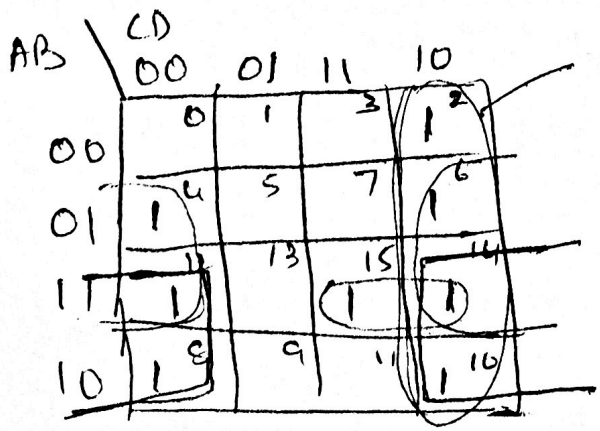
$F_1 = (A, B, C, D) = \sum m(1, 2, 4, 5, 6, 8, 10, 12, 14)$



3 quads
$C\bar{D}$, $B\bar{D}$, $A\bar{D}$
pair $\bar{A}\bar{C}D$

$$F_1 = C\bar{D} + B\bar{D} + A\bar{D} + \bar{A}\bar{C}D$$

$F_2 = (A, B, C, D) = \sum m(2, 4, 6, 8, 10, 12, 14, 15)$



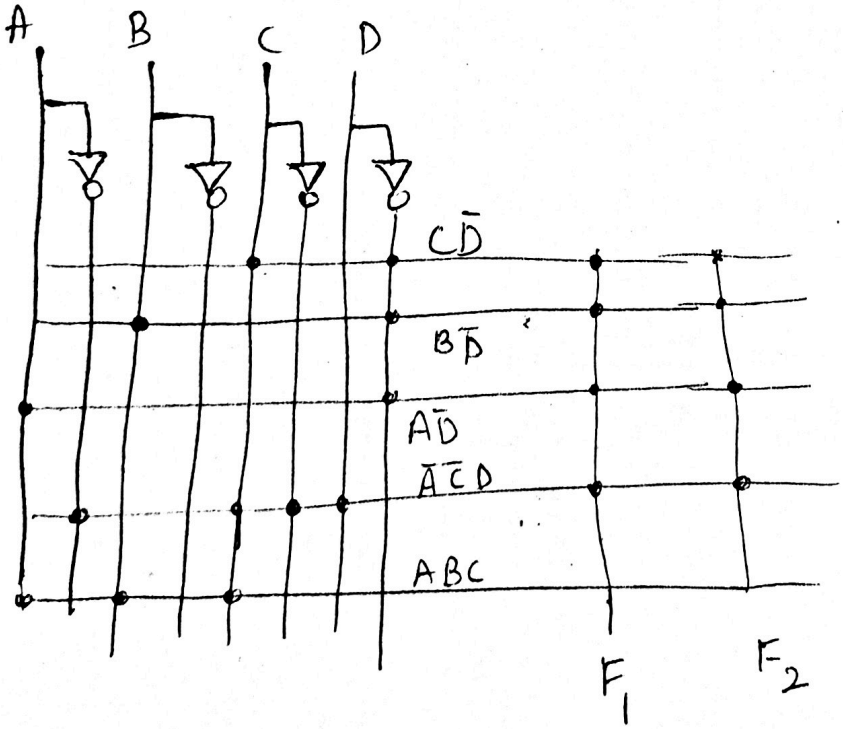
$$F_2 = C\bar{D} + B\bar{D} + A\bar{D} + ABC$$

Unique terms $C\bar{D}$, $B\bar{D}$, $A\bar{D}$, $\bar{A}\bar{C}D$, ABC.

∴ 5 AND gates, two OR for two fn.

PLA table:

Product term	Inputs A B C D	Output F_1 F_2
$C\bar{D}$	- - 1 0	1 1
$B\bar{D}$	- 1 - 0	1 1
$A\bar{D}$	1 - - 0	1 1
$\bar{A}\bar{C}D$	0 - 0 1	1 0
ABC	1 1 1 0	0 1



3a) Excitation table JK, SR - 3marks

Conversion SR to T — 3marks

Excitation tables

SR.

Q	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

JK. F/F Excitable table

Q	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Conversion.

Input	Present state	Next state	Flipflop I/ps	
T	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	1	X	0
1	0	1	1	0
1	1	0	0	1

K-map Simplification

For S

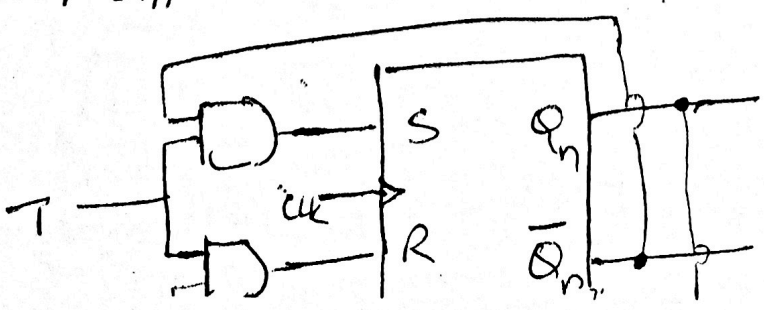
T \ Q_n	0	1
0	0	X
1	1	0

For R

T \ Q_n	0	1
0	X	0
1	0	1

$S = T\,\overline{Q_n}$

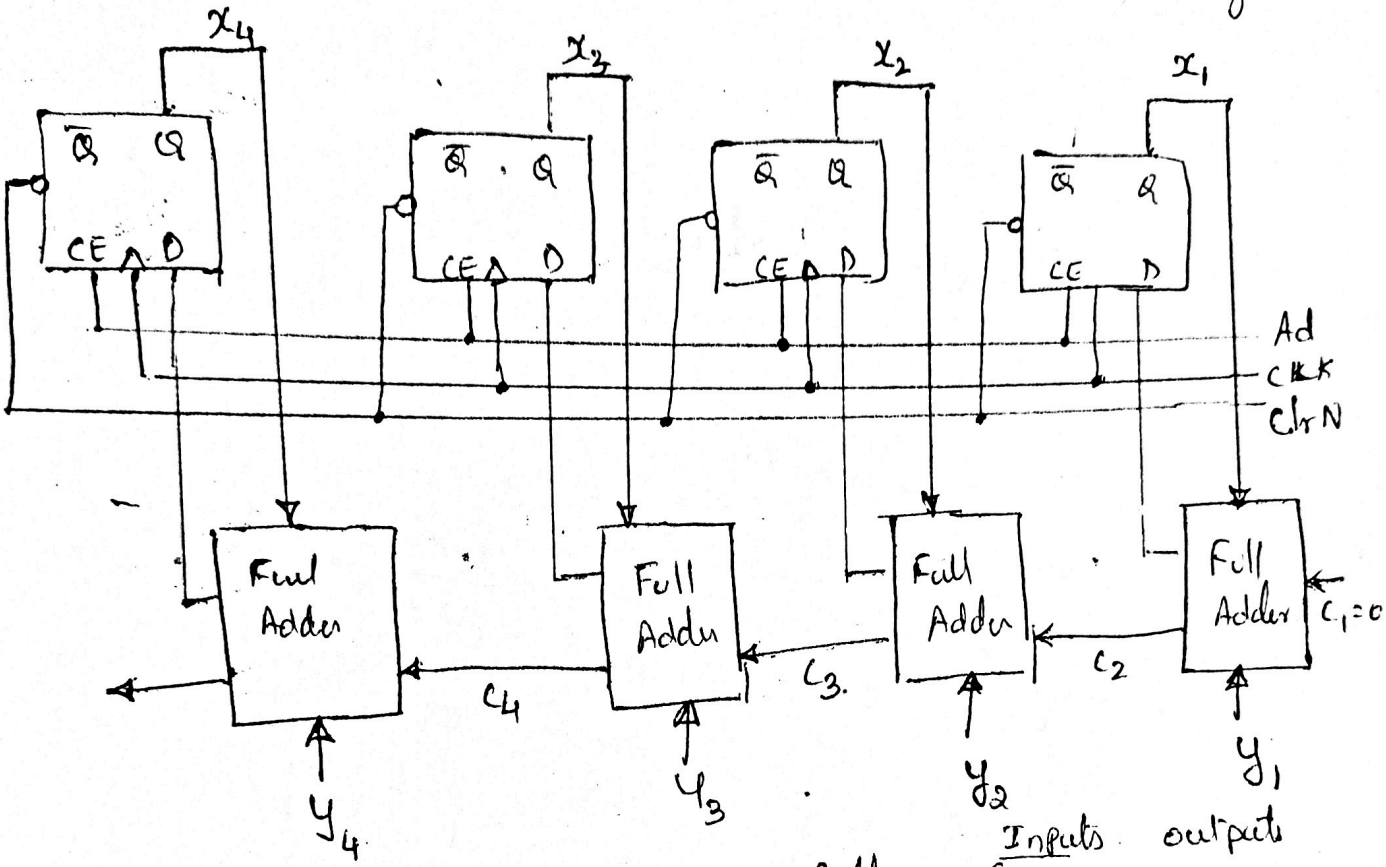
$R = T\,Q_n$



0 ... parallel adder with accumulator (4)

Figure - 2marks

Explan - 2marks



each cell - { fulladder, accumulator F/F

Cell$_i$ -	Inputs	outputs
	C_i	C_{i+1}
	y_i	x_i

1) before addition, accumulator must be loaded with X.

2) carry propagates through adders

4 a.

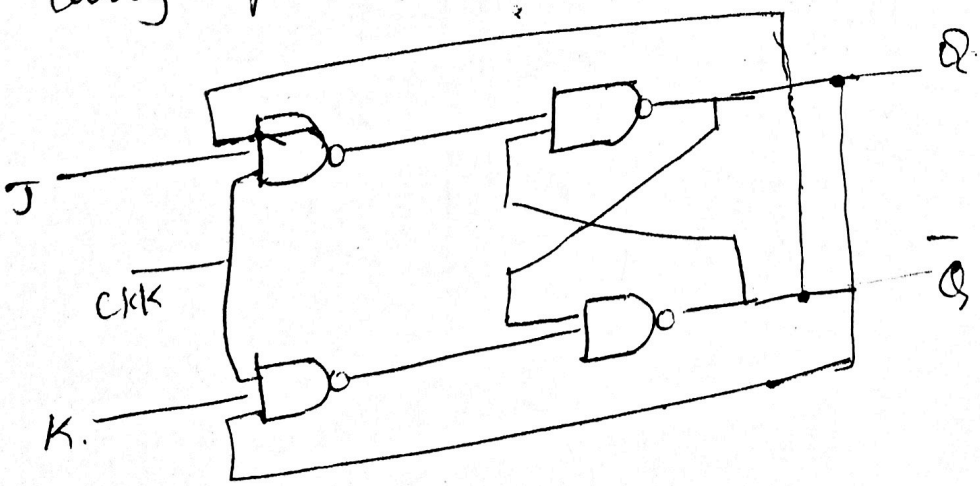


Diagram = 2marks

4marks

1) $J=0$ $K=0$ $Q=0$ $Q=1$

2) $J=0$ $K=\phi$ $Q=0$ $Q=1$

3) $J=1$ $K=0$ $Q=0$ $Q=1$

4) $J=1$ $K=1$ $Q=0$ $Q=1$

4b: Characteristic Equations of SR and JK F/F.

SR. – 2 marks

JK – 2 marks

S	R	Q	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	1	x

S \ RQ	00	01	11	10
0	0	1	0	0
1	1	1	x	x

$$Q_{n+1} = S + \bar{R} Q_n$$

J	K	Q	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

J \ KQn	00	01	11	10
0	0	1	0	0
1	1	1	0	1

$$Q_{n+1} = J \bar{Q}_n + \bar{K} Q_n$$